Actel's Reprogrammable SPGAs

Features

- SRAM-based System Programmable Gate Array (SPGA)
- Efficient silicon target for reusable VHDL and Verilog defined soft blocks
- Fine-grained logic and routing architecture
- 100% automatic placement and routing

High Capacity

- 50,000 to 400,000 usable gates
- Up to 64K embedded dual-port SRAM
- Up to 640 user programmable I/O pins

Highly Predictable Performance

- 75 MHz system performance
- 6ns dual-port SRAM access
- Predictable performance with *MultiDrive* active routing

Systems Design Features

- Supports in-system programming (ISP)
- Multiple *ClockSync* digital phase locked loops provide active delay control for global clock networks
- Up to 16 global clocks and 8 global preset/clear networks
- 5.0V and 3.3V PCI-compliant drivers
- Dual-voltage interface (5V/3.3V)
- Four programmable slew rates per I/O
- *DesignSafe* enables proprietary design protection

Powerful Configuration, Debug and Test Features

- *ActionProbe* provides real-time probing of internal nodes for on-chip debugging
- JTAG support for system-level testability
- Configurable via serial, parallel, or JTAG ports

General Description

Actel's ES family of SPGAs are programmable logic devices designed to address the demand for programmable "systems on a chip". The primary need for high capacity is met by a fine-grained array of logic module blocks, enabling available gate counts from 50,000 gates up to 400,000 gates, made accessible by the unique *MultiDrive* routing hierarchy. This allows designers to achieve unprecedented levels of gate utilization, high levels of performance and performance predictability with 100% automatic place-and-route software. These features makes Actel SPGAs ideal for integrating complex Intellectual Property cores, where meeting design performance goals using large functional blocks synthesized from Verilog or VHDL is essential.

The ES family includes a number of additional features to facilitate its use at the system integration level. The requirement for multiple low-skew clock networks is met by including up to 16 global clock networks and 8 global preset/clear networks. Clock delay control is achieved using multiple on-board *ClockSync* digital phase locked loops. To facilitate remote configuration upgrades, these devices are capable of being reconfigured in the target system. Actel SPGAs are designed as a production solution, featuring support for in-system programmability (ISP) and JTAG. Devices are offered in a variety of industry-standard packages.

Product Profile

Device	A65ES50	A65ES75	A65ES100	A65ES150	A65ES200	A65ES400
Capacity (Logic and SRAM)	50,000	75,000	100,000	150,000	200,000	400,000
Usable Gates						
Minimum	33,000	50,000	66,000	100,000	131,000	263,000
Maximum	84,000	123,000	164,000	250,000	328,000	655,000
Logic Modules						
Sequential (S-MOD3)	2048	3072	4096	6144	8192	16,384
Combinatorial (C-MOD3)	2048	3072	4096	6144	8192	16,384
Combinatorial (C-MOD2)	2048	3072	4096	6144	8192	16,384
SRAM Modules						
RAM Blocks	2	4	8	12	16	32
RAM Bits	4096	8192	16,384	24,576	32,768	65,536
Global Resources						
Clocks	8	8	8	8	16	16
Set/Clear	4	4	4	4	4	4
Data/Control	8	8	8	8	16	16
Digital Phase Lock Loops (DPLL)	2	2	2	2	4	4
User I/O (maximum)	200	240	320	400	480	640
Packages[1]	TQ208	TQ208	TQ208			
	PQ208	PQ208	PQ208			
	PQ240	PQ240	PQ240	RQ240	RQ240	RQ240
	BG240	BG240	BG240	BG240	BG240	BG240
			BG432	BG432	BG432	BG432
			PG391			PG391

Notes:
1. Additional packages will be added.

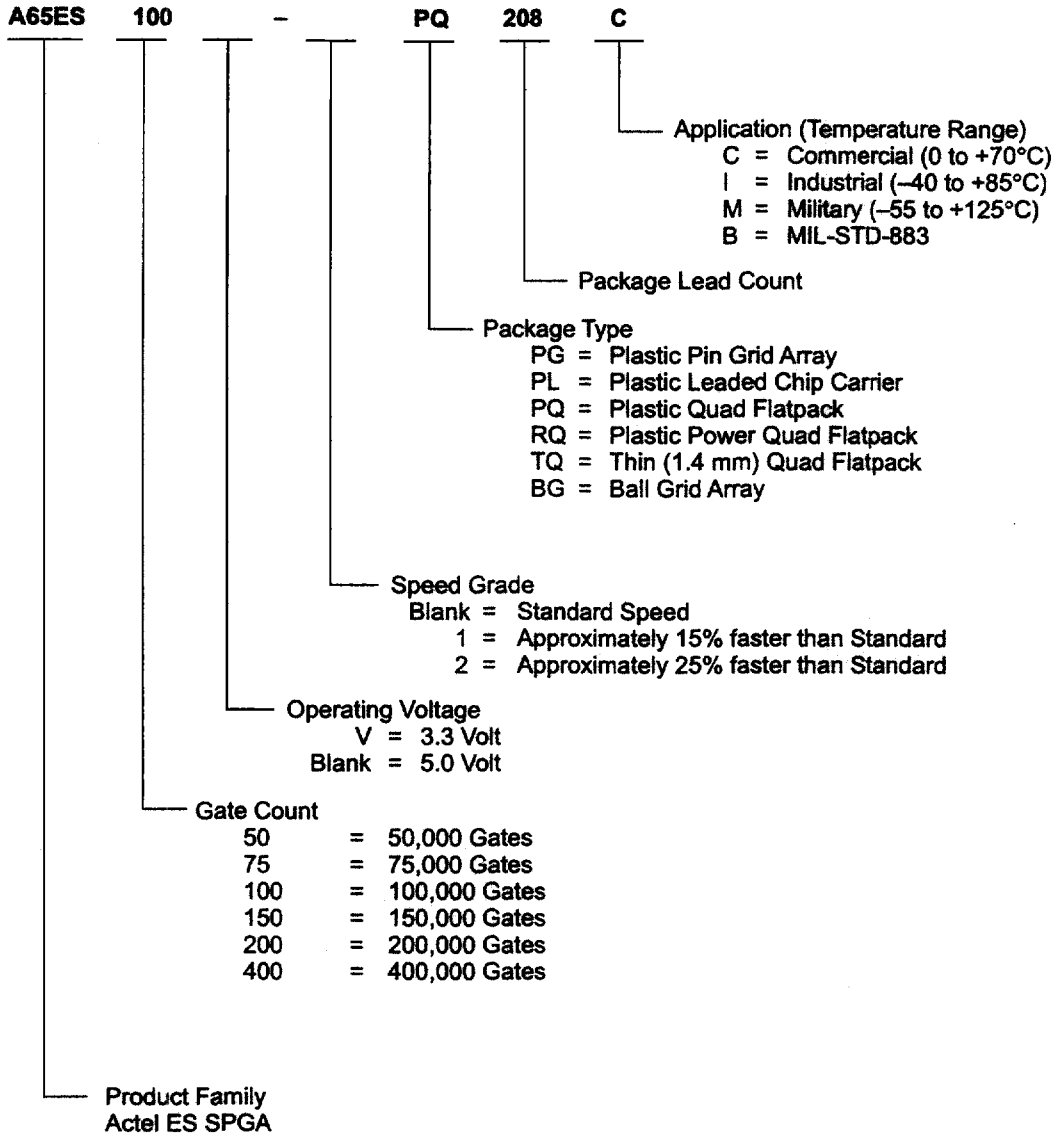
Design Flows

Actel's Designer Series development software supports the ES family by providing a seamless integration into many ASIC design flows. The Designer Series development tools offer automatic placement and routing, static timing analysis, user programming, and debug and diagnostic probe capabilities. In addition, the DirectTime tool provides deterministic and controllable timing. DirectTime allows the designer to specify the performance requirements of individual paths and system clock(s). Using these specifications, the software will automatically optimize logic placement and routing to meet these constraints. Included with the Designer Series tools is Actel's ACTGen™ Macro Builder. ACTGen allows the designer to quickly build fast, efficient logic functions such as counters, adders, FIFOs, and RAM.

The Designer Series tools provide users with the capability to move up to high-level description languages, such as VHDL and Verilog, or use schematic design entry with interfaces to most EDA tools. Designer Series is supported on PC (486 and Pentium) as well as workstation (Sun® and HP®) development platforms. The software provides CAE interfaces to Cadence, Synopsys, Mentor Graphics®, and Viewlogic® design environments. Additional development tools will be supported through Actel's Industry Alliance Program, including DATA I/O (ABEL FPGA) and MINC.

The ES family enables system-level integration capability, merging specialized logic and FPGAs into a single SPGA device. Example applications include DSP, PCI controllers, networking, and telecommunications.

Ordering Information



Product Plan

	Speed Grade			Application			
	Std	–1*	–2*	C	I	M	B
A65ES50 Device							
208-pin Thin Quad Flatpack (TQFP)	P	P	P	P	P	-	-
208-pin Plastic Quad Flatpack (PQFP)	P	P	P	P	P	-	-
240-pin Plastic Quad Flatpack (PQFP)	P	P	P	P	P	-	-
240-pin Super Ball Grid Array (SBGA)	P	P	P	P	P	-	-
A65ES75 Device							
208-pin Thin Quad Flatpack (TQFP)	P	P	P	P	P	-	-
208-pin Plastic Quad Flatpack (PQFP)	P	P	P	P	P	-	-
240-pin Plastic Quad Flatpack (PQFP)	P	P	P	P	P	-	-
240-pin Super Ball Grid Array (SBGA)	P	P	P	P	P	-	-
A65ES100 Device							
208-pin Thin Quad Flatpack (TQFP)	P	P	P	P	P	-	-
208-pin Plastic Quad Flatpack (PQFP)	P	P	P	P	P	-	-
240-pin Plastic Quad Flatpack (PQFP)	✔	✔	P	✔	P	-	-
240-pin Super Ball Grid Array (SBGA)	P	P	P	P	P	-	-
432-pin Super Ball Grid Array (SBGA)	✔	✔	P	✔	P	-	-
391-pin Plastic Pin Grid Array (PPGA)	✔	✔	P	✔	P	-	-
A65ES150 Device							
240-pin Plastic Power Quad Flatpack (RQFP)	P	P	P	P	P	-	-
240-pin Super Ball Grid Array (SBGA)	P	P	P	P	P	-	-
432-pin Super Ball Grid Array (SBGA)	P	P	P	P	P	-	-
A65ES200 Device							
240-pin Plastic Power Quad Flatpack (RQFP)	P	P	P	P	P	-	-
240-pin Super Ball Grid Array (SBGA)	P	P	P	P	P	-	-
432-pin Super Ball Grid Array (SBGA)	P	P	P	P	P	-	-
A65ES400 Device							
240-pin Plastic Power Quad Flatpack (RQFP)	P	P	P	P	P	-	-
240-pin Super Ball Grid Array (SBGA)	P	P	P	P	P	-	-
432-pin Super Ball Grid Array (SBGA)	P	P	P	P	P	-	-
391-pin Plastic Pin Grid Array (PPGA)	P	P	P	P	P	-	-

Applications: *C = Commercial* *I = Industrial* *M = Military* *B = MIL-STD-883*

Availability: ✔ = *Initial* *P = Planned* — = *Not Planned*

* *Speed Grade: –1 = Approx. 15% faster than Standard* *–2 = Approx. 25% faster than Standard*

Actel SPGA Architectural Overview

The ES family has numerous architectural features to aid the system designer. These include:

- Hierarchical, synthesis-friendly logic array optimized for both random logic and datapaths
- Flexible I/O cells
- Fast, dual-port SRAM
- Flexible digital phase lock loops (DPLL) for fine-tuning clock delays

All programmable logic consists of logic units and a routing system that connects these logic units. The structure of the ES architecture can be viewed from either a routing perspective or from a logic perspective. In either case, the ES architecture is conceptually very simple.

The Logic Perspective

The basic logic units in the ES architecture are the S-MOD3, the C-MOD3, and the C-MOD2 illustrated in Figure 1. The C-MOD3 is a function generator that can be configured to be any function of three inputs. The C-MOD2 is also a function generator that can be configured to be any two-input function. The S-MOD3 consists of a C-MOD3 and a D-type flip-flop. When the D flip-flop is not required, its function can be bypassed as shown in Figure 1. Collectively, these three logic modules form the ModuleBlock. The ModuleBlock repeats two dimensionally to create the ES logic array as shown in Figure 2.

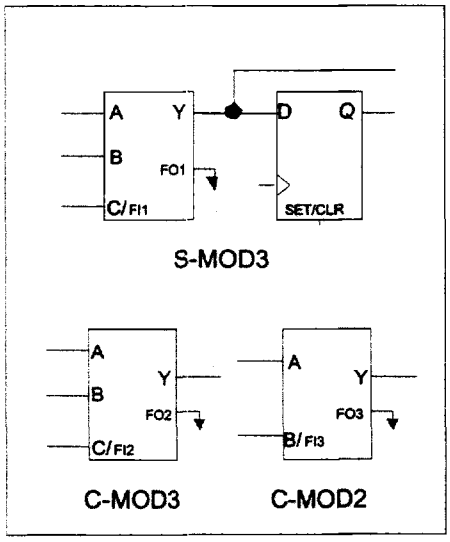


***Figure 1** • The ES family ModuleBlock.*

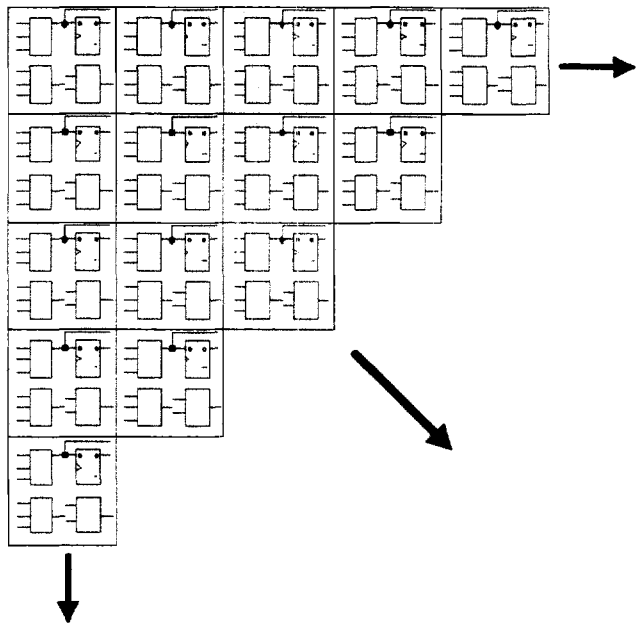


***Figure 2** • Illustration of the sea of ModuleBlocks. The array is replicated in the directions of the arrows.*

The Routing Perspective

The ES family has a multi-tiered routing approach designed to support a tremendous density range of devices. There are two basic categories of routing. The first is local connect providing inter- and intra-ModuleBlock routing. The second is the *MultiDrive* hierarchical expressway system used to drive heavy loads and to transition signals across long spans of logic. Each routing type is defined in Table 1.

The ES family has three types of local routing, the FastConnect, Rt1 (pronounced "root 1") and Rt4. The FastConnect is a high-performance direct connection between modules in adjacent ModuleBlocks. The FastConnect forms a vertical connection path from the top to the bottom of the device, and provides excellent support for datapath functions such as counters, comparators, and adders. The logic inputs and outputs for the FastConnect are illustrated in Figure 1. The functionality of each FOn is equivalent to the module's Y output.

Rt1 and Rt4 are two-dimensional routing meshes which span 1 or 4 ModuleBlocks, respectively. The Rt1 mesh provides connection within and between adjacent blocks for low fanout connections. The Rt4 performs two functions. The first is to support mesh connections within and between the modules in an MBA4 (a 2x2 ModuleBlock Array). The second function is to provide

on/off-ramp access into the hierarchical expressway routing.

The expressway system consists of routing tracks that span distances in a 2^N fashion beginning with Rt16 (see Table 1). This approach repeats hierarchically until the entire device array has been spanned. The expressway system creates logic boundaries or hierarchies. This, coupled with the load-independent *MultiDrive* active routing system, provides excellent delay attributes for long distance connections.

Figure 3 illustrates each of these routing types. The local routing types are superimposed on a group of ModuleBlocks. The first ModuleBlock column illustrates the top-to-bottom orientation of the FastConnect. The next three columns illustrate the Rt1 mesh, and the final four columns show the Rt4 mesh. Note that the Rt4 spans four ModuleBlocks. Above the array, the hierarchical expressway system, including the on/off-ramp function of the Rt4, is shown. The Rt4 directly connects to the output of a module (C-MOD3 for example), which can then connect with any expressway level using its on-ramp capability. Once the required distance has been traversed, the off-ramp provides connection back down to the inputs of the driven modules. Expressways run both vertically and horizontally.

Enhanced Performance through Active Routing

Actel has taken a fresh approach to the routing hierarchy. The local mesh still handles most of the net routing. At higher levels, however, there are two major differences. First, a continuum of routing resources provide a very close match to the minimum-length routing segment needed for any net. In addition, drive capability is associated with expressway-level routing resources. This "active routing" approach not only provides automatic buffering of long nets (freeing the designer of design analysis to add buffers), but also makes the array very predictable. Table 1 shows the delay associated with routing tracks spanning lengths from four to 128 ModuleBlocks.

***Table 1** • Routing types in ES.*

Type	Name	Function	ModuleBlock Span	Boundary Limit	Delay (ns)[1]
Direct	FastConnect[3]	Local High Performance	N/A	None	0.8
Mesh	Rt1	Inter- and Intra-ModuleBlock	1	None	2.0
Mesh/Bridge	Rt4	Local Mesh and On/Off Ramp	2x2	None	2.3
Hierarchical Expressways	Rt16	DataSlice Input[2]	4x4	MBA16	3.9
	Rt64		8x8	MBA64	4.6
	Rt256		16x16	MBA256	5.5
	Rt1K		32x32	MBA1K	7.1
	Rt4K		64x64	MBA4K	9.0
	Rt16K		128x128	MBA16K	12.0

Notes:

1. *Delay is worst case commercial for a -1 speed grade and includes a C-MOD3 delay.*
2. *The special inputs of the DataSlice, CLK, RESET, and DS1/DS2, are only accessible through the Rt64 tracks and global resources.*
3. *The FastConnect links the FO output to the FI input of C-MODs and S-MODs.*

Synthesis

The various architectural features, both logic and routing, are designed to enhance synthesis support. The granular nature of the C-MOD3 and C-MOD2 can be easily manipulated by synthesis tools to generate random logic and state machines. Datapath functions are supported through structured logic builders such as Actel's ACTgen and the Synopsys DesignWare tool. Hierarchical active routing also improves the timing model, limiting the architectural knowledge a synthesis tool requires to effectively map to the ES family.

Global Resources

There are three types of global resources in the ES family: clock, preset/clear, and general-purpose. Each of these resources can be driven by an external pin or by an internal function. The global signals are distributed throughout the device down to the level of the DataSlice, a 16-ModuleBlock structure, which is illustrated in Figure 4. The DataSlice has four inputs which can be accessed via the global resources The CLKx input pins are connected to the CLK input of the DataSlice. The PCLx input pins are connected to the RESET input of the DataSlice. The GDIx input pins are connected to both the DS1 and DS2 inputs of the DataSlice. Local connections to the four DataSlice inputs can also be made using the Rt64 expressways.

The DataSlice is important to understand for two reasons. The first is that the DataSlice creates the baseline granularity for sequential functions because the CLK and RESET inputs are common to all 16 registers in the DataSlice. The second is that the DS1 and DS2 inputs provide powerful resources for controlling and manipulating large datapath logic, since the DataSlice is a natural building block for datapath-oriented logic. Although the DataSlice concept is important to understand, architectural features associated with it are handled transparently by the Designer Series software.

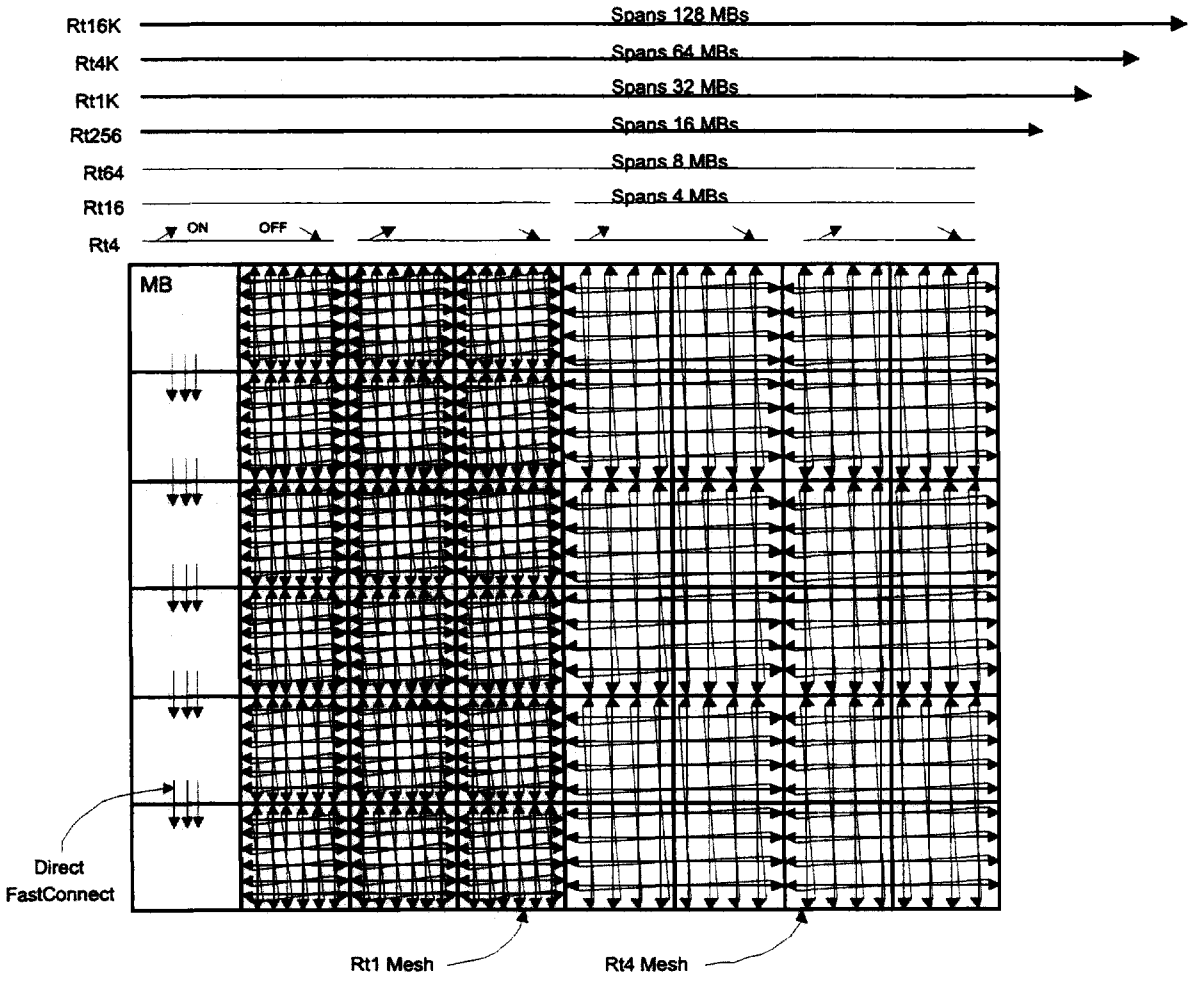


Figure 3 • Illustration of routing mechanisms. Each bold square represents one ModuleBlock.

For more on the use of global resources, see the "Using Global Resources" application note.

Enhanced Clock Delay Control through Digital Phase Locked Loop (DPLL)

The *ClockSync* feature uses Digital Phase Locked Loop (DPLL) technology to enhance clock delay control for

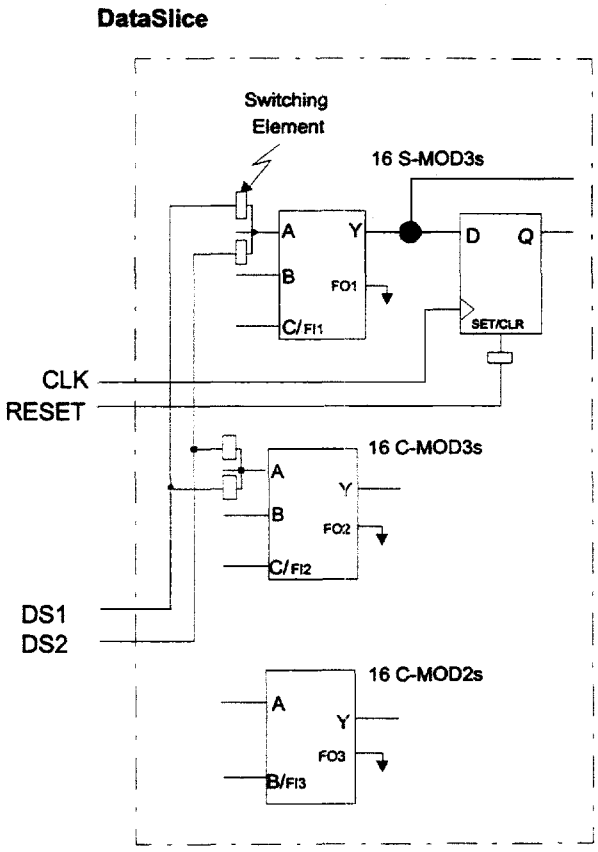


Figure 4 • DataSlice structure.

improved system performance. *ClockSync* is extremely flexible, allowing CLK-Q (pad-pad) manipulation from 14ns down to 0ns. The DPLL has three coarse-delay modes (STD, SP1, and SP2) in addition to an 800ps-per-increment user-programmable mode to support a wide range of delays.

The DPLL has a maximum jitter of 300ps at worst-case commercial conditions and consumes 400µW/MHz. In addition, Actel's DPLL implementation can be turned off and restarted without significant impact to the system.

Application Note: See *Digital Phase Lock Loop Usage* for more information.

Flexible Interfacing with Programmable I/O

The ES family provides a range of I/O options to match the most demanding high-performance interface requirements. Programmable options for I/O pads include the following:

- Four-level slew rate control from 3V/ns down to 1V/ns at 35pF loading
- Both 3.3V and 5V PCI-compliant drivers
- Input buffer and output power control
- Input buffer threshold level and delay
- Output polarity control
- Output enable polarity control

In addition, the ES family can operate in a 5V system, a 3.3V system, or mixed-voltage systems. Three separate Vcc supply networks are provided on the chip: two for the I/O ring and one for the array core. The I/O ring can be driven with a single supply or two different (e.g., 3.3v and 5v) supplies. The array core can be driven with either voltage. Level translators are provided to accommodate all possible combinations of voltage levels for the input and output signals. Inputs are 5V tolerant even if the device is configured to be a 3.3V-only device. See Table 2 for additional information.

Table 2 • System voltage flexibility. See power and ground pin descriptions for more details on each voltage configuration.

	3.3V Array	5.0V Array
3.3V I/O	Supported[1]	Supported[1,2]
5.0V I/O	Supported[3]	Supported

Notes:
1. *Inputs can be configured to be 5V tolerant.*
2. *This mode supports enhanced array performance in a 3.3V I/O requirement system.*
3. *Option for lower power consumption with 5V drive requirement.*

Application Note: See *Using I/O Circuits in the ES Family* for complete data on programmable options.

Enhanced Flexibility with On-Board SRAM

ES devices contains SRAM divided into 2K-bit blocks. Each block is a dual-port (one read port, one write port) structure as shown in Figure 5. The SRAM can be organized in a variety of ways as shown in Table 3. The SRAM supports high-performance applications by providing a maximum access time of 6 ns for synchronous read operations and 10ns for asynchronous operations.

The ES family SRAM modules are true dual-port embedded blocks containing independent READ and WRITE ports. Each SRAM module contains eight bits of read and write addressing (RDAD[7:0] and WRAD[7:0] respectively) to support 256x8-bit blocks. In addition, three high-order decodes, WEN[2:0] and REN[2:0], are provided for multi-block RAM requirements. The read and write ports of the SRAM block contain independent clocks (RCLK and WCLK) with programmable polarities, offering active HIGH or LOW implementation. The SRAM block contains eight data inputs (WD[7:0]) and eight data outputs (RD[7:0]). The read data outputs can be three-stated using the FOE[2:0] control lines to provide

higher-performance read operations for multi-block RAM operations. The ES dual-port SRAM blocks are ideal for high-speed buffered applications requiring fast FIFO and LIFO queues. Actel's ACTGen Macro Builder provides the capability to quickly design memory functions, such as FIFOs, LIFOs, and RAM arrays. Additionally, unused SRAM blocks need not be wasted since they can be used to implement registers, look-up tables, and ROM for other applications within the design.

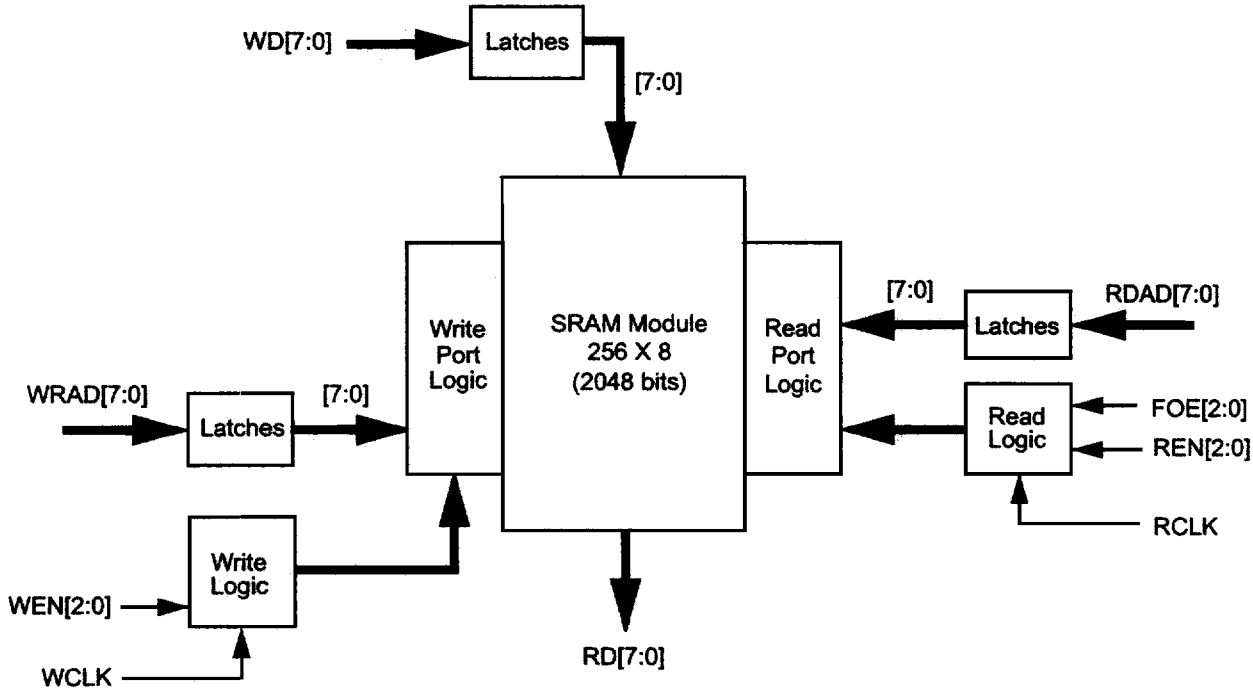


Figure 5 • Dual-Port SRAM Block

Table 3 • SRAM Configuration Options

Data Width	SRAM Organizations
x8	256x8,512x8, 768x8,1024x8
x16	256x16,512x16
x24	256x24
x32	256x32

Pin Descriptions

Global Signals

Each global resource can be accessed by an input pin or by an internal source. The global resources can also remain unused. When an internal function drives a global resource, the pin normally associated with the global function can still be used as an output pin. If the global function is unused, the pin can act as an I/O.

CLKx Clock (input)
Global clock inputs.

PCLx Preset/Clear (Input)
Global preset/clear input.

GDIx Globally-Distributed Input (Input)
Special global inputs which can be used for any data or control function.

Standard Inputs and Outputs

I/O Input/Output (Input, Output)
An I/O pin can function as an input, output, three-state or bi-directional buffer. Input and output levels are selectable. Unused I/O pins are configured as outputs driving LOW (i.e., to ground) by the Designer Series software.

NC No Connection
This pin is not connected to circuitry within the device.

Configuration and Test Pins

The following pins are used to configure the device. Dedicated pins cannot be used as I/O. All other pins are

multiplexed function, and will return to the I/O state following the end of configuration.

M0,M1,M2 Mode (Input)

The three Mx pins define the device configuration mode. These are dedicated configuration pins.

CONn Configuration (Input/Output)

This open-drain pin initiates configuration. Configuration starts on the first CCLK edge after CONn goes LOW and continues until the configuration is complete. The device will resume normal operation a few clock cycles after CONn goes high. Dedicated configuration pin.

CSn Configuration Chip Select In (Input)

This pin is used in conjunction with CSOUTn to select a device in the cascade configuration mode. It is driven LOW and held LOW when the device is being actively configured. Dedicated configuration pin.

CCLK Configuration Clock (Input or Output)

This pin is an input or an output depending on the configuration mode. When it is an output, it is derived from the on-chip oscillator.

CSOUTn Configuration Chip Select Out (Output)

This pin is used in conjunction with CSn to select a device in the cascade configuration mode. The device drives it LOW and holds it LOW when a downstream device is being actively configured.

FRAME_CLK Frame Clock(Output)

This pin provides a pulse at each byte boundary during parallel or serial configuration modes. The FRAME_CLK will go high when the all configuration requirements are complete.

ERRORn Error (Output)

This open-drain pin signals an error during configuration. It also serves as the output of the checking operation during check mode.

D(7:0) Configuration Data (Input)

Configuration data for parallel transfer modes. Serial configuration requires only D0.

A(18:0) Configuration Address (Output)

Provides address to PROM during configuration cycles.

TCK JTAG Test Clock (input)

Clock signal to shift the JTAG data into the device. This pin functions as an I/O when the JTAG mode is not selected.

TDI JTAG Test Data In (Input)

Serial data input for JTAG instructions and data. Data is shifted in on the rising edge of TCK. This pin functions as an I/O when the JTAG mode is not selected.

TDO JTAG Test Data Out (Output)

Serial data output for JTAG instructions and test data. This pin functions as an I/O when the JTAG mode is not selected.

TMS JTAG Test Mode Select (Input)

Serial data input for JTAG test mode. Data is shifted in on the rising edge of TCK. This pin functions as an I/O when the JTAG mode is not selected.

PROBE Probe(Output)

The probe pin is used to output data from any user-defined design node within the device. This independent diagnostic pin allows real-time diagnostic output of any signal within the device. The probe pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

Power and Ground

V_{CCA} Array Supply Voltage (Input)

Input supply voltage for the internal array.

V_{CCH} Higher I/O Supply Voltage (Input)

One of two input supply voltage inputs for the I/O ring. In a single-voltage system, V_{CCH} and V_{CCL} are connected together. In a two-supply system, V_{CCH} is connected to the higher voltage. V_{CCH} defines the allowable voltage threshold for inputs.

V_{CCL} Lower I/O Supply Voltage (Input)

One of two input supply voltage inputs for the I/O ring. In a single-voltage system, V_{CCH} and V_{CCL} are connected together. In a two-supply system, V_{CCL} is connected to the lower voltage. V_{CCL} defines the drive level for outputs.

GND Ground (Input)

Input LOW supply voltage.

Device Programming Options

This section briefly describes ES configuration modes and the resources needed to implement them. For more detailed information, refer to the "Configuring ES Devices" application note.

Configuration Modes

There are seven configuration modes and one *Reset* mode for the ES family. The pins M2, M1 and M0 define the various mode. A logic '0' is typically implemented by tying the appropriate mode pin to the system ground. A logic '1' is implemented by tying to an external pull-up resistor. The *Reset* mode is automatically entered upon power-up or by pulling the dedicated pins M2, M1, and

M0 low. The ES device is ready for configuration once power-up is complete and the mode pins are in a valid configuration mode (1-7). The ES family supports both *Master* and *Slave* configuration modes.

In *Master* mode, the configuration clock is generated by the ES device and output on the CCLK pin. In *Slave* mode, the configuration clock is supplied externally to the CCLK pin or the JTAG TCK pin.

Table 4 • Configuration modes.

Mode	M[2:0]	Clock	Data	Addressing
1	001	Slave	Parallel	Count-up
2	010	Slave	Parallel	Count-down
3	011	Slave	Serial	NA
4	100	Master	Serial	NA
5	101	Master	Parallel	Count-up
6	110	Slave	Parallel	Peripheral
7	111	Slave	Serial[1]	NA

Notes:
1. *JTAG configuration mode.*

Configuration data is applied to the ES device either in *parallel* (8 bits at a time) or *serial* (1 bit at a time) format. For parallel configuration, an address is supplied to the external configuration EPROM by either the ES device or a peripheral device. The ES device generates sequential count-up or count-down addresses. For the serial configuration modes, only the CCLK and D0 pins are required.

Multiple ES devices can be configured by the same external configuration device in *Cascade* mode. Refer to the Application Note "Configuring ES Devices" for a more detailed description on implementing the various configuration modes.

Configuration Resources

There are five dedicated configuration pins (M2, M1, M0, CSn, CONn). Depending on the configuration mode, up to 29 dual-function pins are required. Once configuration is complete, dual-function pins become available as I/O.

Configuration Time

The configuration time for the ES family varies by device. The initial device, the A65ES100 will take approximately 300ms to complete configuration in both the serial and parallel modes.

Design Security

The ES family offers a special security feature, *DesignSafe*, to prevent reverse engineering of the design; however, this mechanism does not prevent design replication. The configuration data stream must first be encrypted by the Designer Series software. The device is then able to automatically detect encryption and unscramble the bit stream to correctly configure the device. Designer provides no "unscramble" mechanism, thus providing design security.

Table 5 • Number of pins required for each configuration mode.

Mode	Dedicated Pins	Required Pins	Optional Pins[5]	Notes
1	5	28	3	1
2	5	28	3	1
3	5	2	3	2
4	5	2	3	2
5	5	28	3	1
6	5	9	3	3
7	5	4	2	4

Notes:
1. *The required pins are CCLK, A(18-0), and D(7-0)*
2. *The required pins are CCLK and D0.*
3. *The required pins are CCLK and D(7-0).*
4. *Requires the four JTAG pins (TCK, TMS, TDI, and TDO).*
5. *The optional pins are FRAME_CLK, CSOUTn and ERRORn. The CSOUTn is not required for Mode 7.*

Test Circuitry

The ES family provides the means to test and debug a design once it is configured into a device. These devices contain Actel's *ActionProbe*® test facility. Once a device has been configured, *ActionProbe* allows the designer to probe any internal node during device operation to aid in debugging a design. In addition, ES devices contain JTAG 1149.1 Boundary Scan Test.

JTAG Boundary Scan Testing (BST)

Device pin spacing is decreasing with the advent of fine-pitch packages such as TQFP and BGA packages, and manufacturers are routinely implementing surface-mount technology with multi-layer PC boards. Boundary scan is becoming an attractive tool to help systems manufacturers test their PC boards. The Joint Test Action Group (JTAG) developed the IEEE Boundary Scan standard 1149.1 to facilitate board-level testing during manufacturing.

IEEE Standard 1149.1 defines a 4-pin Test Access Port (TAP) interface for testing integrated circuits in a system. The ES family provides four JTAG BST pins: Test Data In (TDI), Test Data Out (TDO), Test Clock (TCK), and Test Mode Select (TMS). Devices are configured in a JTAG "chain" where BST data can be transmitted serially between devices via TDO to TDI interconnections. The

TMS and TCK signals are shared between all devices in the JTAG chain so that all components operate in the same state.

The ES family implements a subset of the IEEE 1149.1 Boundary Scan Test (BST) instruction, in addition to a private instruction to allow the use of Actel's *Actionprobe* with JTAG BST. Refer to the IEEE 1149.1 specification for detailed information regarding JTAG testing.

JTAG Architecture

The ES JTAG BST circuitry consists of a Test Access Port (TAP) controller, JTAG instruction register, JPROBE register, bypass register and boundary scan register. Figure 6 is a block diagram of the ES JTAG circuitry.

When a device is operating in JTAG BST mode, four I/O

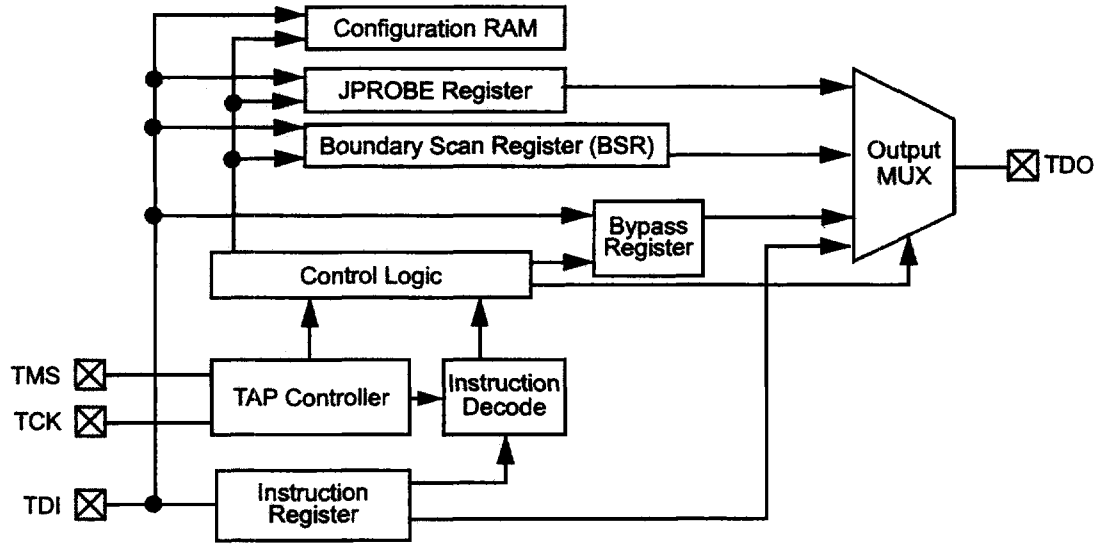


Figure 6 • JTAG BST Circuitry

pins are used for the TDI, TDO, TMS, and TCK signals. An active reset (nTRST) pin is not supported; however, the ES family contains power-on-reset circuitry which resets the JTAG BST circuitry upon power-up. During normal device operation, the JTAG pins TDI and TMS hold be held HIGH to disable the JTAG circuitry. The following table summarizes the functions of the JTAG BST signals.

JTAG Signal	Name	Function
TDI	Test Data In	Serial data input for JTAG instructions and data. Data is shifted in on the rising edge of TCK.
TDO	Test Data Out	Serial data output for JTAG instructions and test data.
TMS	Test Mode Select	Serial data input for JTAG test mode. Data is shifted in on the rising edge of TCK.
TCK	Test Clock	Clock signal to shift the JTAG data into the device.

JTAG BST Instructions

JTAG BST testing within the ES device is controlled by a Test Access Port (TAP) state machine. The TAP controller drives the four-bit instruction register, a bypass register, and the boundary scan data registers within the device. The TAP controller uses the TMS signal to control the JTAG testing of the device. The JTAG test mode is determined by the bit stream entered on the TMS pin. Table 6 describes the JTAG instructions supported by the ES family of devices.

ActionProbe

After a device has been successfully configured, any internal logic or I/O module output can be observed using the ActionProbe circuitry and the PROBE output pin. ActionProbe provides the software and hardware required to perform real-time debugging. During dynamic operation the internal node is addressed using the JTAG input pins (TCK, TMS, and TDI). Once addressed, the internal node is mapped to the probe pin for observation and debug.

Table 6 • JTAG instruction codes.

Test Mode	Code	Selected Register(s)	Description
EXTEST	0000	BSR	Allows the external circuitry and board-level interconnections to be tested by driving outputs to known values and capturing input values.
SAMPLE/ PRELOAD	0001	BSR	Provides dynamic capture and data load capability used with the EXTEST command.
INTEST	0010	BSR	Refer to IEEE 1149.1 Specification
SILSIG ID CODE	0011	JPROBE[2]	An instruction used to read both the 32-bit ID code (manufacturer, device, etc.) and the 32-bit user defined code (silicon signature). The silicon signature is defined by the user when generating the programming sequence for the device. This information is loaded into the JPROBE register during the Capture_DR state and scanned out TDO during the Shift_DR state.
USER INSTRUCTION	0100	User Defined	This instruction allows the user to build data register using the programmable logic by delivering TDI, CLKDR, SHIFTDR, and UPDTDR to the core and receiving TDO from the user scan chain.
ActionProbe	0101	JPROBE	ActionProbe function. The internal address is loaded into the JPROBE register during the Shift_DR state. Once this is complete, the internal node will be mapped dynamically to the PROBE output pin.
Reserved	0110	Bypass	
Parallel Probe	0111	JPROBE	Instruction providing the ability to scan out all logic information in the device. The information is loaded into the JPROBE register 64-bits at a time during the Capture_DR state and scanned out TDO during the Shift_DR state.
Reserved	10XX	Bypass	
CLAMP	1100	Bypass	Refer to IEEE 1149.1 Specification
HIGH Z	1101	Bypass	Refer to IEEE 1149.1 Specification
JTAG Programming	1110	Bypass and Configuration RAM	This instruction is used to program the device via the JTAG inputs for Mode 7 configuration. After power up, the device will be waiting for the JTAG controller to enter the Shift-DR stated and to sequentially clock in data. The data is routed through the Bypass register but is also tapped into the data input for the configuration RAM. Other devices which share the same scan chain on the board should be put in the Bypass mode to guarantee the success of programming.
BYPASS	1111	Bypass	Enables the bypass register between the TDI and TDO pins. The test data passes through the selected device to adjacent devices in the JTAG chain.

Notes:

1. *BSR is the Boundary Scan Register.*
2. *JPROBE is an 85-bit register consisting of the Internal_Address_Register (21 bits) and the Probe_Register (64 bits).*

Masked Array Program

Actel will continue its popular masked array program with the ES family. The masked array program offers significant cost reductions for high volume applications. Please contact your local Actel sales representative for more information

Operating Conditions

Absolute Maximum Ratings

Symbol	Parameter	Limits	Units
V_{CCA}	Array Supply Voltage	-0.5 to 7.0	V
V_{CCH}	I/O High Supply Voltage	-0.5 to 7.0	V
V_{CCL}	I/O Low Supply Voltage[3]	-0.5 to 7.0	V
V_I	Input Voltage	–0.5 to V_{CCH}+0.5	V
V_O	Output Voltage	–0.5 to V_{CCH}+0.5	V
I_{IO}	I/O Source/Sink Current[2]	±20	mA
T_{STG}	Storage Temperature	–65 to +150	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.*
2. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than V_{CC} + 0.5 V or less than GND – 0.5 V, the internal protection diode will be forward biased and can draw excessive current.*
3. *The value of V_{CCL} must not exceed the value of V_{CCH}.*

Recommended Operating Conditions

Parameter	Commercial	Industrial	Units
Temperature Range[1]	0 to +70	–40 to +85	°C
V_{CCA} Range[2]	3.15 to 5.25	3.0 to 5.5	V
V_{CCH} Range[2]	3.15 to 5.25	3.0 to 5.5	V
V_{CCL} Range[2,3]	3.15 to V_{CCH}	3.0 to V_{CCH}	V

Note:

1. *Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.*
2. *V_{CCA}, V_{CCH}, and V_{CCL} are functional across the defined range; however, the propagation delays in the data sheet are limited to the standard 3.3V and 5.0V ranges. Also, the devices should be operational down to 2.2V; however, this is not a tested parameter.*
3. *The value of V_{CCL} must not exceed the value of V_{CCH}.*

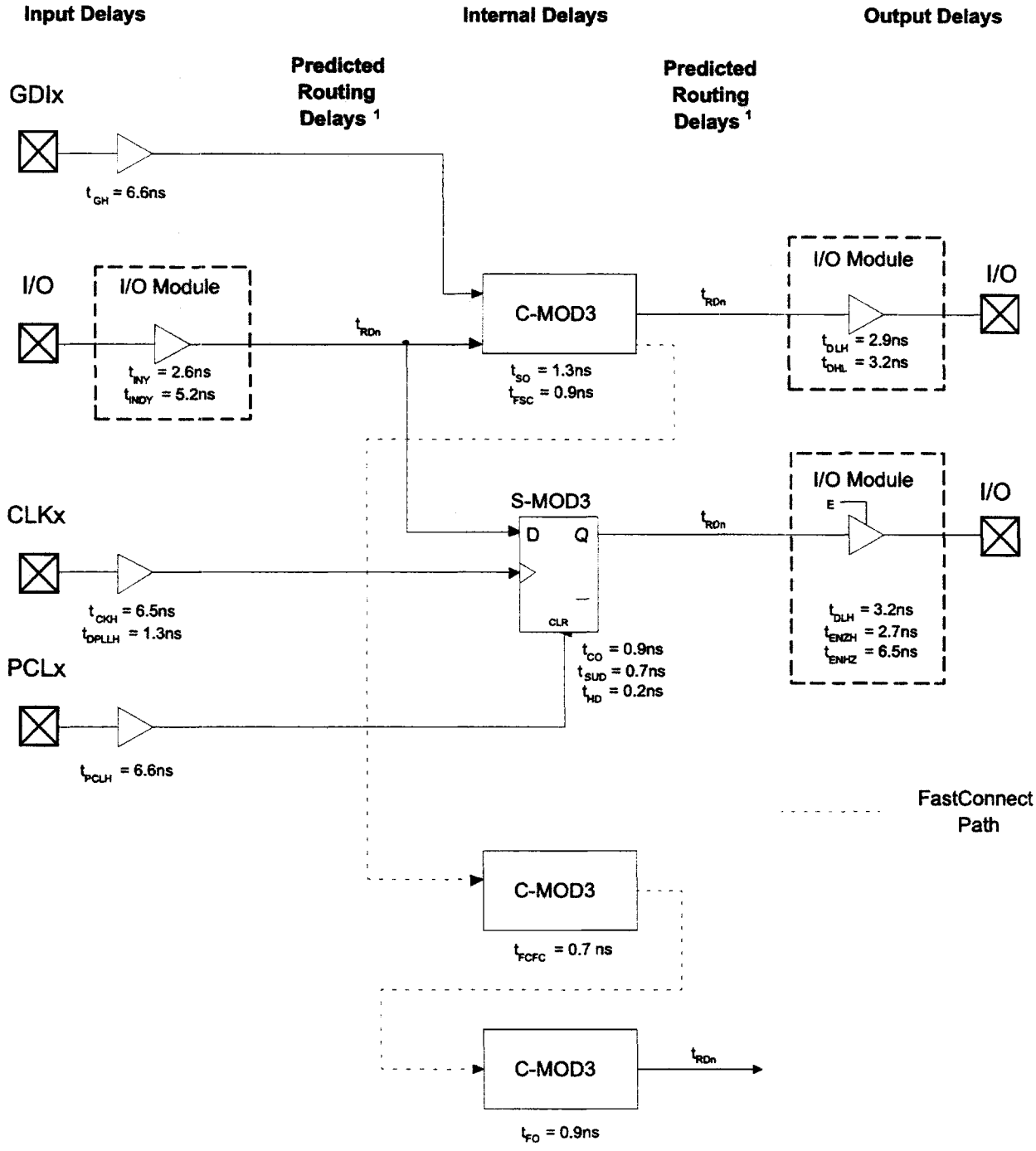
Electrical Specifications

Symbol	Parameter	Commercial/Industrial		Units
		Min.	Max.	
V_{OH}[1]	Output High (@ I_{OH} = -6mA)	3.84		V
V_{OL}[1]	Output Low (@ I_{OL} = 6mA)		0.33	V
V_{IL}	Low Input (TTL)	–0.3	0.8	V
	Low Input (CMOS)	-0.3	V_{CCL}/2 - 0.15	V
V_{IH}	High Input (TTL)	2.0	V_{CCH}+0.3	V
	High Input (CMOS)	V_{CCL}/2 + 0.15	V_{CCH}+0.3	V
t_R, t_F[2]	Input Transition Time		500	ns
C_{IO}[2, 3]	I/O Capacitance		10	pF
I_{CCS}[4]	Standby Current at 5V Operation		100	µA

Notes:

1. *Only one output tested at a time. V_{CC} = minimum for 5V operation.*
2. *Not tested, for information only.*
3. *Includes worst-case 391 PPGA package capacitance. V_{OUT} = 0 V, f = 1 MHz.*
4. *All outputs unloaded. All inputs = V_{CC} or GND.*

Timing Model

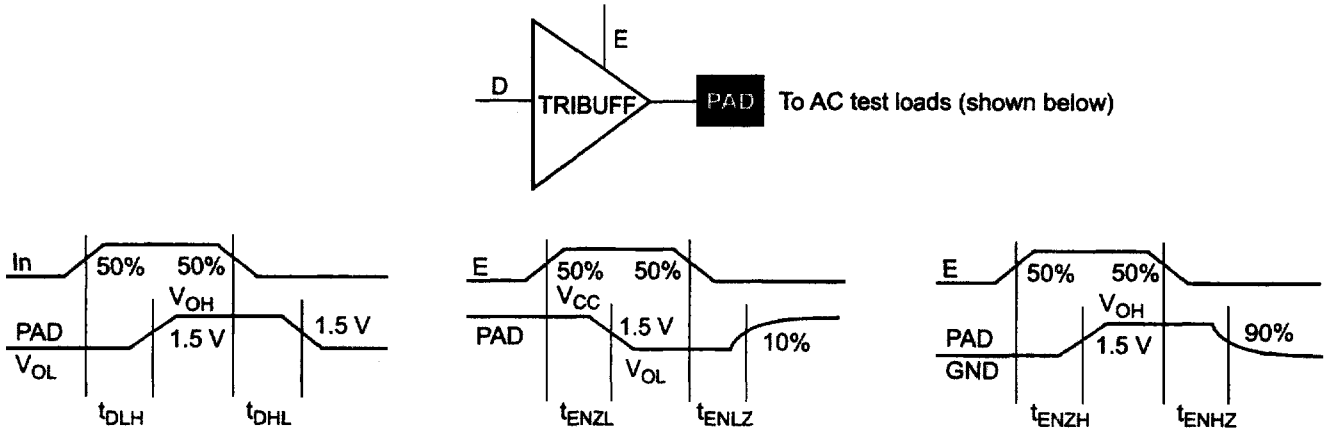


Notes:

1. *The t_{RDn} delays are t_{RD1} = 0.7ns, t_{RD2} = 0.9ns, t_{RD4} = 1.4ns, and t_{RD8} = 2.6ns for loads of 1, 2, 4, and 8 respectively.*
2. *All delays shown are worst case commercial using a -1 speed grade.*

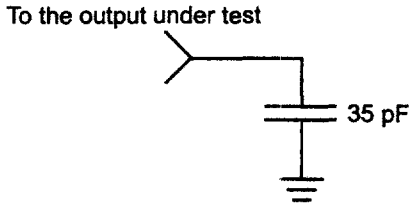
Parameter Measurement

Output Buffer Delays

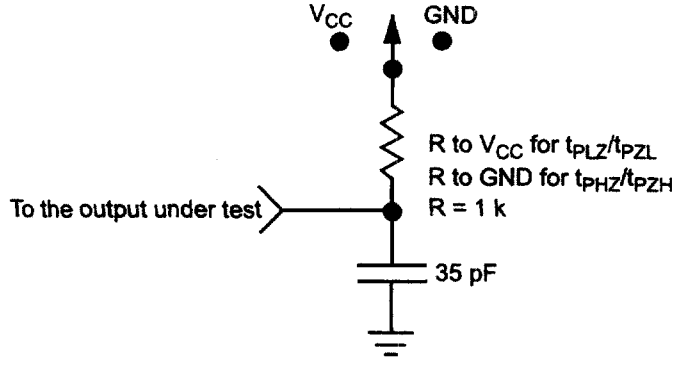


AC Test Loads

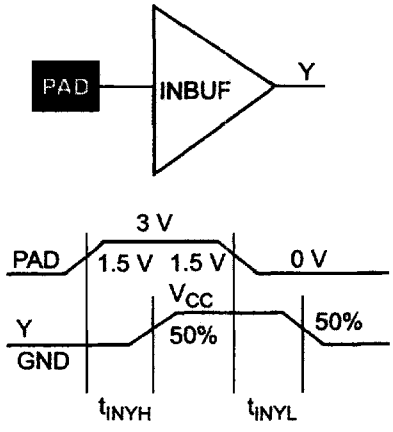
Load 1
(Used to measure propagation delay)



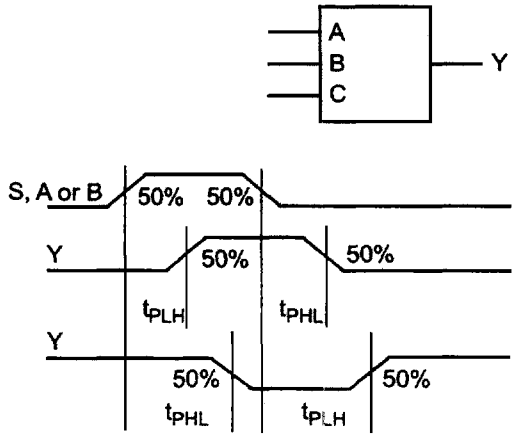
Load 2
(Used to measure rising/falling edges)



Input Buffer Delays

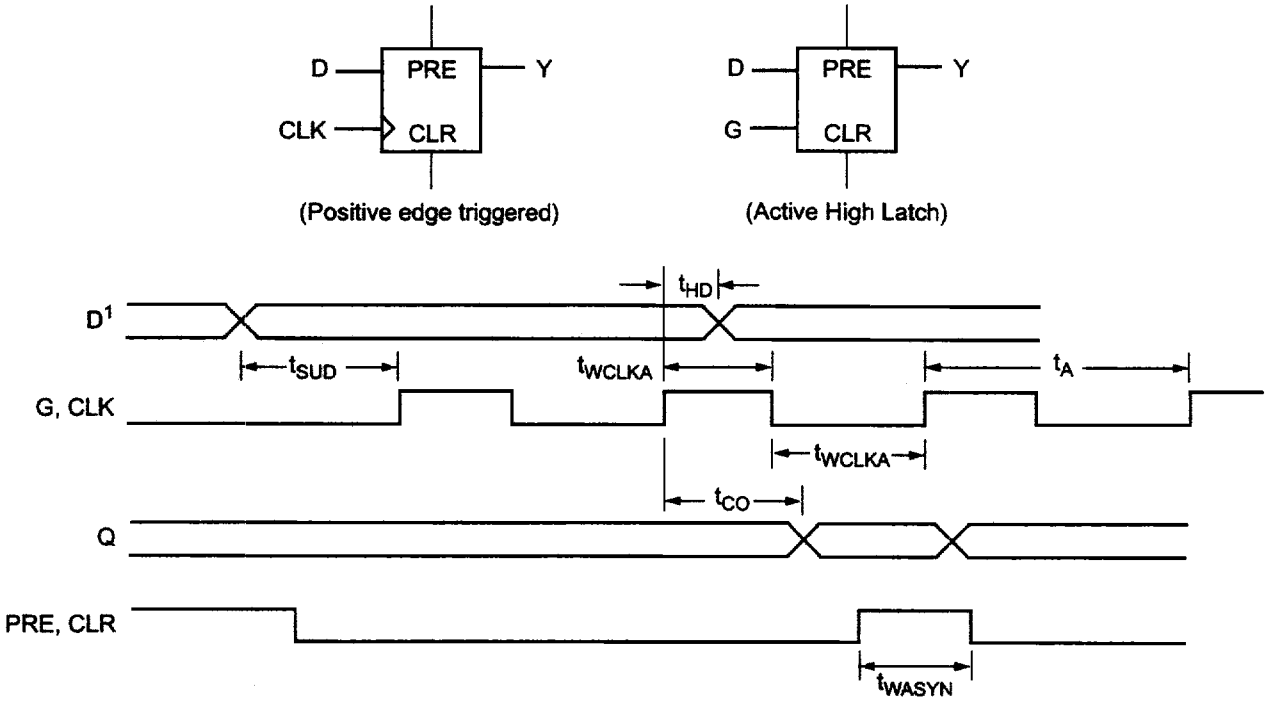


Module Delays



Sequential Module Timing Characteristics

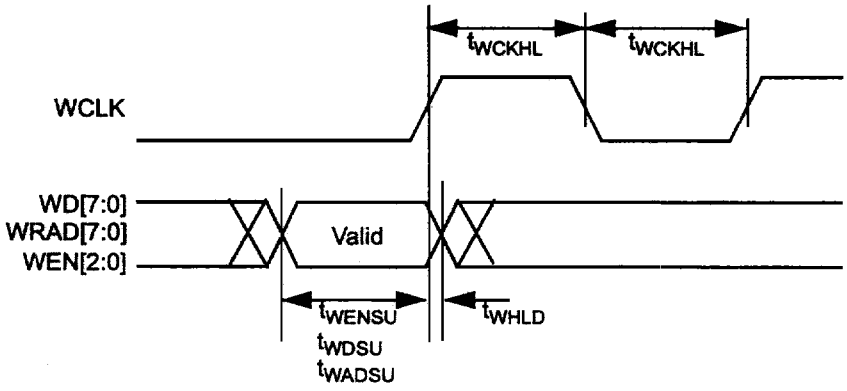
Flip-Flops and Latches



Note: D represents all data functions involving A, B, and C for S-MOD3 flip-flops.

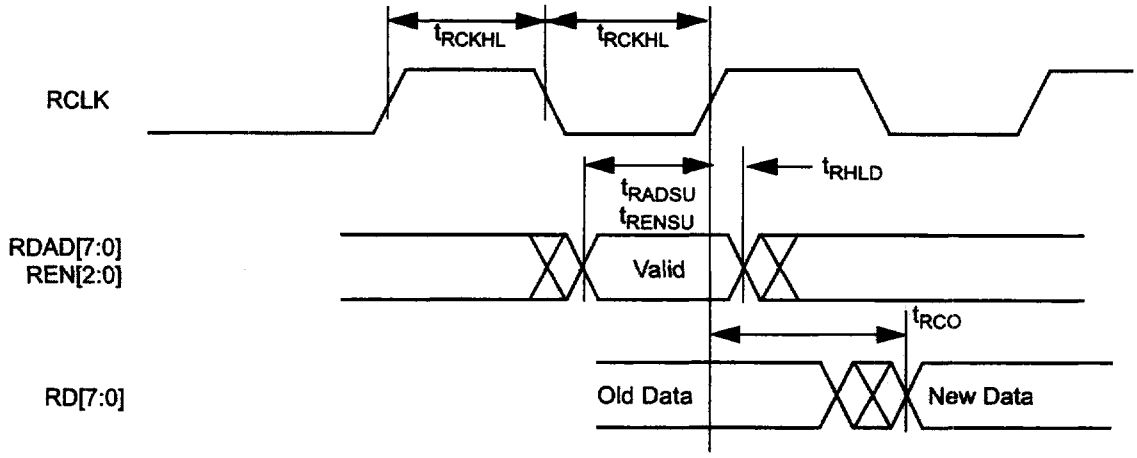
SRAM Timing Characteristics

ES Family SRAM Write Operation



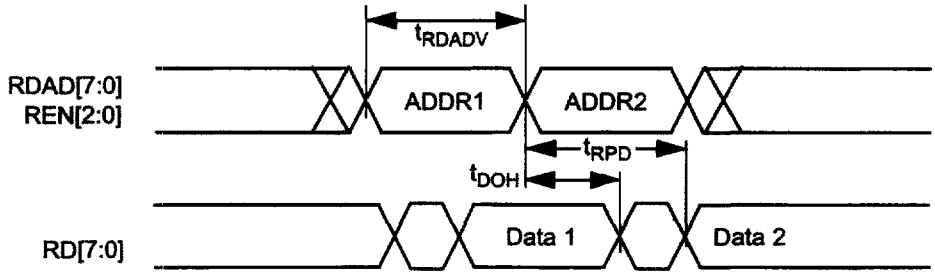
Note: Identical timing for falling-edge clock.

ES Family SRAM Synchronous Read Operation

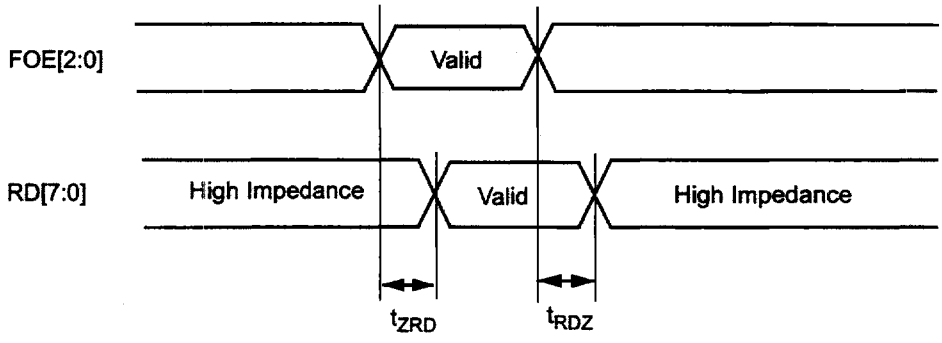


Note: Identical timing for falling-edge clock.

ES Family SRAM Asynchronous Read Operation



High Impedance Read Operation Timing



Timing Characteristics

Timing characteristics for devices fall into two categories: fixed and design dependent. Fixed delays include input and output buffers, global resources, and logic module delays. Internal routing delays are device-dependent. Design dependency means actual delays are not determined until after the design's placement and routing is complete. Delay values may then be determined by using the Designer Series utility or performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets which are used for initial design performance evaluation. Since the architecture provides deterministic timing and abundant routing resources, Actel's Designer Series development tools offer DirectTime, a timing-driven place and route tool. Using DirectTime, the designer may specify timing-critical nets and system clock frequency. Using these specifications, the place and route software optimizes the layout of the design to meet the user's specifications.

Expressways

Some nets in the design will use the longer expressways. This additional delay is represented statistically in higher fanout (FO=8) routing delays in the data sheet specifications section.

Timing Derating

The delay tables on the following pages are expressed in terms of worst-case commercial operating conditions for each supported speed grade. To obtain typical commercial, industrial, or military, use the appropriate multiplier found in the table of standard derating factors. Additional derating factors are provided in the "Complete Temperature and Voltage Derating Factors" table for the worst-case process. To obtain the best-case process derating factor, multiply the worst-case factor by 0.45.

External Sequential Timing

Table 7 defines approximate external sequential timing characteristics for the ES family using both regular and DPLL adjusted clocks. The parameters are input setup, input hold and output CLK-Q and were calculated with the following assumptions:

- An input buffer (INBUF) directly feeds an S-MOD3 with a routing delay of 1ns.
- An S-MOD3 directly feeds an output buffer (OUTBUF) with a routing delay of 1ns.

Table 7 • Approximate external sequential timing for an A65ES100-1 device at commercial conditions.

Clock Type	Input Setup	input Hold	CLK-Q
Regular	0ns[1]	<1ns[1]	12
Regular	-2ns	3ns	12
DPLL[2]	3ns	0ns	7

Notes:

1. *INBUF delay option used.*
2. *The clock can be further offset, positively or negatively, in increments of 800ps. Additional modes are available to further enhance CLK-Q delays. See the "Using the DPLL" application note for more information.*

Standard Range Derating Factors (Temperature, Voltage, and Process)

	Commercial			Industrial		Military	
	Best	Typical	Worst	Best	Worst	Best	Worst
Derating Multiplier	0.35	0.85	1.00	0.31	1.11	0.30	1.23

Complete Temperature and Voltage Derating Factors for 5.0V and 3.3V Operation

	–55	–40	0	25	70	85	125
V_{CC}-10%	0.75	0.79	0.86	0.92	1.06	1.11	1.23
V_{CC}-5%	0.71	0.75	0.82	0.87	1.00	1.05	1.16
V_{CC}	0.69	0.72	0.80	0.85	0.97	1.02	1.13
V_{CC}+5%	0.68	0.69	0.77	0.82	0.95	0.98	1.09
V_{CC}+10%	0.67	0.69	0.76	0.81	0.93	0.97	1.08

Note: Normalized to Worst-Case Commercial: V_{CC} = 4.75V or 3.15V, T_J, 70°C, Worst Process

A65ES100 Timing Characteristics

(Worst-Case Commercial Conditions, V_{CC} = 4.75 V, T_J = 70°C)

Logic Module Propagation Delays		'-2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Standard Module Delays[1]								
t_{SO}	Single Module - Standard In to Out		1.1		1.3		1.5	ns
t_{CO}	Sequential Clk to Q		0.8		0.9		1.0	ns
t_{GO}	Latch G to Q		0.8		0.9		1.0	ns
t_{RS}	Flip-Flop Asynchronous Reset to Q		1.1		1.3		1.5	ns
Predicted Routing Delays[2]								
t_{RD1}	FO=1 Routing Delay		0.6		0.7		0.8	ns
t_{RD2}	FO=2 Routing Delay		0.8		0.9		1.1	ns
t_{RD4}	FO=4 Routing Delay		1.3		1.4		1.7	ns
t_{RD8}	FO=8 Routing Delay		2.3		2.6		3.0	ns
FastConnect Delays[1]								
t_{SFC}	Standard In to FastConnect Out		0.8		0.9		1.1	ns
t_{FCFC}	FastConnect In to FastConnect Out		0.7		0.8		0.9	ns
t_{FO}	FastConnect Input to Standard Out		0.8		0.9		1.1	ns
Sequential Timing Characteristics[3]								
t_{SUD}	Flip-Flop (Latch) Data Input Setup	1.7		2.0		2.2		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	2.3		2.6		3.0		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	2.3		2.6		3.0		ns
t_A	Flip-Flop Clock Input Period	7.5		8.5		10.0		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		130		120		100	MHz

Notes:

1. *A predicted routing delay should be added to all standard module delays and to t_{FO} to obtain the complete path delay.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-MOD3. Timing is measured from the data inputs, A, B, or C, of the S-MOD3. Timing parameters for sequential elements not based on the S-MOD3 are routing dependent and timing should be verified in post-layout timing tools.*

A65ES100 Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

I/O Module Propagation Delays (Standard Inputs)		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Pad to Y High		2.3		2.6		3.0	ns
t_{INYL}	Pad to Y Low		1.9		2.1		2.5	ns
t_{INDYH}	Pad to Delayed Y High		4.6		5.2		6.1	ns
t_{INDYL}	Pad to Delayed Y Low		4.2		4.8		5.6	ns
Input Module Predicted Routing Delays[1]								
t_{RD1}	FO=1 Routing Delay		0.6		0.7		0.8	ns
t_{RD2}	FO=2 Routing Delay		0.8		0.9		1.1	ns
t_{RD4}	FO=4 Routing Delay		1.3		1.4		1.7	ns
t_{RD8}	FO=8 Routing Delay		2.3		2.6		3.0	ns
Global Clock Network (Standard Clock)								
t_{CKH}	Input Low to High		5.7		6.5		7.6	ns
t_{CKL}	Input High to Low		5.3		6.0		7.0	ns
t_{PWH}	Minimum Pulse Width High	2.3		2.6		3.0		ns
t_{PWL}	Minimum Pulse Width Low	2.3		2.6		3.0		ns
t_{CKSW}	Maximum Skew		1.5		1.5		1.5	ns
Global Clock Network (using DPLL)[2]								
t_{DPLH}	Input Low to High		1.1		1.3		1.5	ns
t_{DPHL}	Input High to Low		0.8		0.9		1.0	ns
t_{PWH}	Minimum Pulse Width High	2.3		2.6		3.0		ns
t_{PWL}	Minimum Pulse Width Low	2.3		2.6		3.0		ns
t_{CKSW}	Maximum Skew		1.5		1.5		1.5	ns
t_{CKJ}	DPLL Jitter		230		250		300	ps
t_{CKD}	DPLL Frequency Range	20	100	20	100	20	100	MHz
Globally-Distributed Inputs								
t_{GLH}	Input Low to High		5.9		6.6		7.8	ns
t_{GHL}	Input High to Low		5.9		6.6		7.8	ns
Global Presets/Clears								
t_{PCLH}	Input Low to High		5.9		6.6		7.8	ns
t_{PCHL}	Input High to Low		5.9		6.6		7.8	ns

Note:

1. *These parameters should be used for estimating device performance. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
2. *Timing for the "STD" DPLL mode only with default programmable offset. See the "Digital Phase Lock Loop Usage" application note for more information on user-programmable offset and the special modes.*

A65ES100 Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

I/O Module Timing (Outputs)		'-2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Timing[1]								
t_{DLH}	Data to Pad High		2.0		2.3		2.7	ns
t_{DHL}	Data to Pad Low		3.4		3.8		4.5	ns
t_{ENZH}	Enable Pad Z to High		2.0		2.2		2.6	ns
t_{ENZL}	Enable Pad Z to Low		3.0		3.4		4.0	ns
t_{ENHZ}	Enable Pad High to Z		5.7		6.5		7.6	ns
t_{ENLZ}	Enable Pad Low to Z		5.5		6.2		7.3	ns
d_{TLH}	Capacitive Loading, Low to High		0.02		0.03		0.03	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.03		0.03		0.04	ns/pF
CMOS/PCI Output Timing[1]								
t_{DLH}	Data to Pad High		2.6		2.9		3.4	ns
t_{DHL}	Data to Pad Low		2.9		3.2		3.8	ns
t_{ENZH}	Enable Pad Z to High		2.4		2.7		3.2	ns
t_{ENZL}	Enable Pad Z to Low		2.3		2.6		3.1	ns
t_{ENHZ}	Enable Pad High to Z		5.7		6.5		7.6	ns
t_{ENLZ}	Enable Pad Low to Z		5.5		6.2		7.3	ns
d_{TLH}	Capacitive Loading, Low to High		0.02		0.03		0.03	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.02		0.03		0.03	ns/pF

Notes:

1. Delays based on 35 pF loading using fastest slew driver.

RAM Timing Table (continued)

(Worst case commercial conditions)

		Advanced Information						
Logic Module Timing		**'–2 Speed**		**'–1' Speed**		**'Std' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
SRAM Write Operations								
t_{WCKHL}	Write Clock High/Low Time	1.5		1.7		2.0		ns
t_{WADSU}	Write Address Setup Time	1.1		1.3		1.5		ns
t_{WDSU}	Write Data Setup Time	0.8		0.9		1.0		
t_{WENSU}	Write Enable Setup Time	1.5		1.7		2.0		
t_{WHLD}	Write Address/Data/Enable Hold	0.5		0.5		0.5		ns
SRAM Synchronous Read Operations								
t_{RCKHL}	Read Clock High/Low Time	4.5		5.1		6.0		ns
t_{RCO}	Read Data Valid After Clock High/Low		5.2		6.0		7.0	ns
t_{ADSU}	Read Address Setup Time	1.1		1.3		1.5		ns
t_{RENSU}	Read Enable Setup	1.5		1.7		2.0		ns
t_{RHLD}	Read Address/Enable Hold	0.5		0.5		0.5		ns
SRAM Asynchronous Read Operations								
t_{RPD}	Asynchronous Access Time		6.8		7.6		9.0	ns
t_{RDADV}	Read Address Valid Time	6.8		7.6		9.0		ns
t_{DOH}	Data Out Hold Time	1.0		1.0		1.0		ns
t_{RDZ}	Read Data to High Impedance		1.5		1.7		2.0	ns
t_{ZRD}	High Impedance to Read Data Valid		1.5		1.7		2.0	ns

A65ES100 Timing Characteristics

(Worst-Case Commercial Conditions, V_{CC} = 3.0 V, T_J = 70°C)

Logic Module Propagation Delays		'-2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Standard Module Delays[1]								
t_{SO}	Single Module - Standard In to Out		1.6		1.8		2.2	ns
t_{CO}	Sequential Clk to Q		1.1		1.2		1.4	ns
t_{GO}	Latch G to Q		1.1		1.2		1.4	ns
t_{RS}	Flip-Flop Asynchronous Reset to Q		1.6		1.8		2.2	ns
Predicted Routing Delays[2]								
t_{RD1}	FO=1 Routing Delay		0.9		1.0		1.2	ns
t_{RD2}	FO=2 Routing Delay		1.2		1.3		1.6	ns
t_{RD4}	FO=4 Routing Delay		1.8		2.1		2.4	ns
t_{RD8}	FO=8 Routing Delay		3.2		3.7		4.3	ns
FastConnect Delays[1]								
t_{SFC}	Standard In to FastConnect Out		1.2		1.3		1.6	ns
t_{FCFC}	FastConnect In to FastConnect Out		1.0		1.1		1.3	ns
t_{FO}	FastConnect Input to Standard Out		1.2		1.3		1.6	ns
Sequential Timing Characteristics[3]								
t_{SUD}	Flip-Flop (Latch) Data Input Setup	2.4		2.7		3.2		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.2		3.7		4.3		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	3.2		3.7		4.3		ns
t_A	Flip-Flop Clock Input Period	10.8		12.2		14.4		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		93		82		70	MHz

Notes:

1. *A predicted routing delay should be added to all standard module delays and to t_{FO} to obtain the complete path delay.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-MOD3. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*

A65ES100 Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

I/O Module Propagation Delays (Standard Inputs)		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Pad to Y High		3.2		3.7		4.3	ns
t_{INYL}	Pad to Y Low		2.7		3.1		3.6	ns
t_{INDYH}	Pad to Delayed Y High		6.6		7.5		8.8	ns
t_{INDYL}	Pad to Delayed Y Low		6.0		6.9		8.1	ns
Input Module Predicted Routing Delays[1]								
t_{RD1}	FO=1 Routing Delay		0.9		1.0		1.2	ns
t_{RD2}	FO=2 Routing Delay		1.2		1.3		1.6	ns
t_{RD4}	FO=4 Routing Delay		1.8		2.1		2.4	ns
t_{RD8}	FO=8 Routing Delay		3.2		3.7		4.3	ns
Global Clock Network (Standard Clock)								
t_{CKH}	Input Low to High		8.2		9.3		10.9	ns
t_{CKL}	Input High to Low		7.6		8.6		10.1	ns
t_{PWH}	Minimum Pulse Width High	3.2		3.7		4.3		ns
t_{PWL}	Minimum Pulse Width Low	3.2		3.7		4.3		ns
t_{CKSW}	Maximum Skew		1.5		1.5		1.5	ns
Global Clock Network (using DPLL)[2]								
t_{DPLH}	Input Low to High		1.6		1.8		2.2	ns
t_{DPHL}	Input High to Low		1.1		1.2		1.4	ns
t_{PWH}	Minimum Pulse Width High	3.2		3.7		4.3		ns
t_{PWL}	Minimum Pulse Width Low	3.2		3.7		4.3		ns
t_{CKSW}	Maximum Skew		1.5		1.5		1.5	ns
t_{CKJ}	DPLL Jitter		320		350		430	ps
t_{CKD}	DPLL Frequency Range	20	100	20	100	20	100	MHz
Globally-Distributed Inputs								
t_{GLH}	Input Low to High		8.6		9.8		11.5	ns
t_{GHL}	Input High to Low		8.1		9.2		10.8	ns
Global Presets/Clears								
t_{PCLH}	Input Low to High		8.6		9.8		11.5	ns
t_{PCHL}	Input High to Low		8.1		9.2		10.8	ns

Note:

1. *These parameters should be used for estimating device performance. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
2. *Timing for the "STD" DPLL mode only with default programmable offset. See the "Digital Phase Lock Loop Usage" application note for more information on user-programmable offset and the special modes.*

A65ES100 Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

I/O Module Timing (Outputs)		'-2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Timing[1]								
t_{DLH}	Data to Pad High		2.9		3.3		3.9	ns
t_{DHL}	Data to Pad Low		4.9		5.5		6.5	ns
t_{ENZH}	Enable Pad Z to High		2.8		3.2		3.7	ns
t_{ENZL}	Enable Pad Z to Low		4.3		4.9		5.8	ns
t_{ENHZ}	Enable Pad High to Z		8.2		9.3		10.9	ns
t_{ENLZ}	Enable Pad Low to Z		7.9		8.9		10.5	ns
d_{TLH}	Capacitive Loading, Low to High		0.03		0.04		0.04	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.04		0.05		0.06	ns/pF
CMOS/PCI Output Timing[1]								
t_{DLH}	Data to Pad High		3.7		4.2		4.9	ns
t_{DHL}	Data to Pad Low		4.1		4.7		5.5	ns
t_{ENZH}	Enable Pad Z to High		3.5		3.9		4.6	ns
t_{ENZL}	Enable Pad Z to Low		3.3		3.8		4.5	ns
t_{ENHZ}	Enable Pad High to Z		8.2		9.3		10.9	ns
t_{ENLZ}	Enable Pad Low to Z		7.9		8.9		10.5	ns
d_{TLH}	Capacitive Loading, Low to High		0.03		0.04		0.04	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.03		0.04		0.04	ns/pF

Notes:

1. Delays based on 35 pF loading using fastest slew driver.

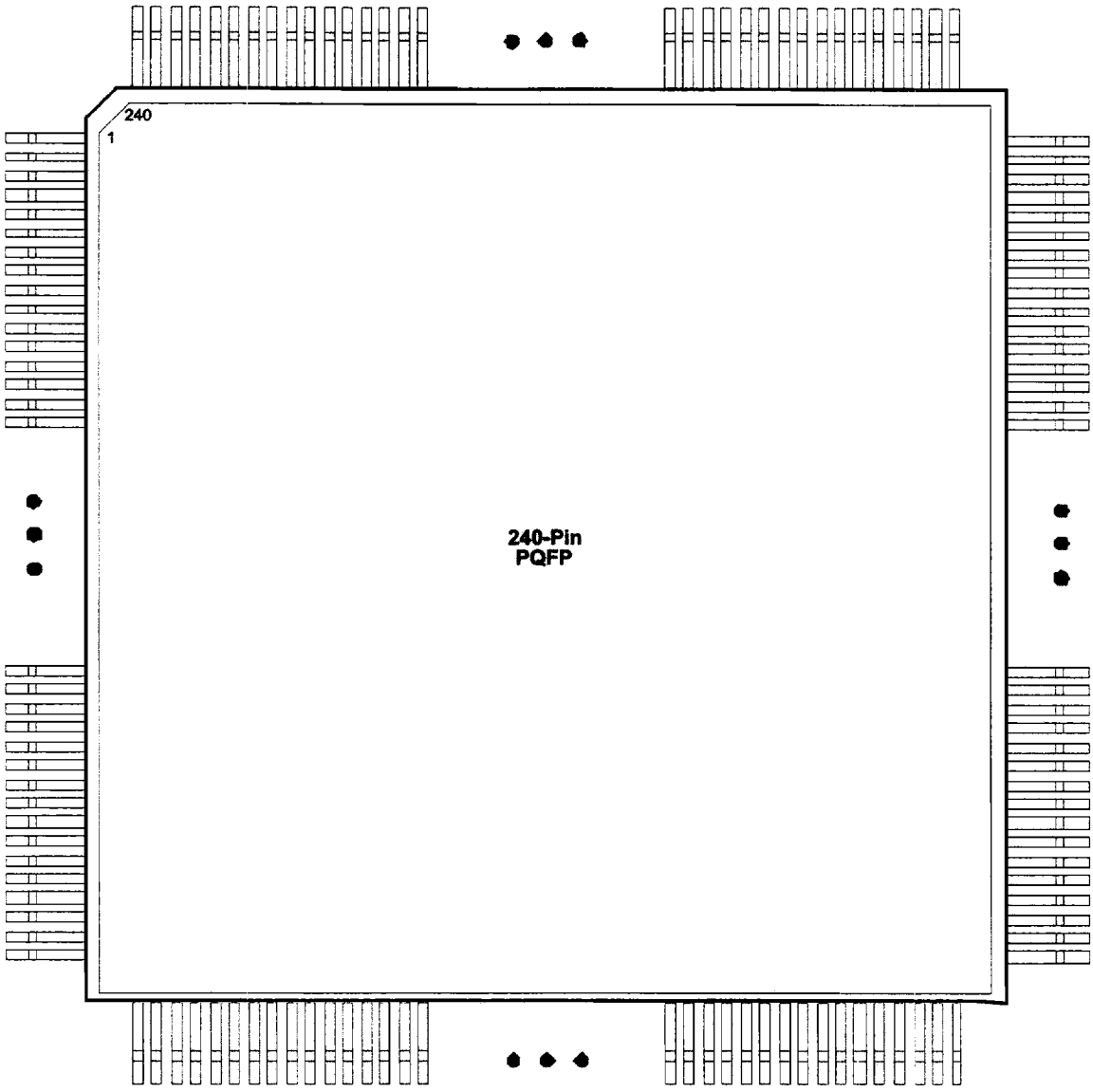
RAM Timing Table (continued)

(Worst case commercial conditions)

		Advanced Information						
Logic Module Timing		**'–2 Speed**		**'–1' Speed**		**'Std' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
SRAM Write Operations								
t_{WCKHL}	Write Clock High/Low Time	2.2		2.4		2.9		ns
t_{WADSU}	Write Address Setup Time	1.6		1.9		2.2		ns
t_{WDSU}	Write Data Setup Time	1.2		1.3		1.4		
t_{WENSU}	Write Enable Setup Time	2.2		2.4		2.9		
t_{WHLD}	Write Address/Data/Enable Hold	0.7		0.7		0.7		ns
SRAM Synchronous Read Operations								
t_{RCKHL}	Read Clock High/Low Time	6.5		7.3		8.6		ns
t_{RCO}	Read Data Valid After Clock High/Low		7.5		8.6		10.1	ns
t_{ADSU}	Read Address Setup Time	1.6		1.9		2.2		ns
t_{RENSU}	Read Enable Setup	2.2		2.4		2.9		ns
t_{RHLD}	Read Address/Enable Hold	0.7		0.7		0.7		ns
SRAM Asynchronous Read Operations								
t_{RPD}	Asynchronous Access Time		9.8		10.9		13.0	ns
t_{RDADV}	Read Address Valid Time	9.8		10.9		13.0		ns
t_{DOH}	Data Out Hold Time	1.4		1.4		1.4		ns
t_{RDZ}	Read Data to High Impedance		2.2		2.4		2.9	ns
t_{ZRD}	High Impedance to Read Data Valid		2.2		2.4		2.9	ns

Package Pin Assignments

240-Pin PQFP Package (Top View)



Notes:

1. *NC: Denotes No Connection*
2. *All unlisted pin numbers are user I/Os*
3. *M0, M1, and M2 must be terminated to GND or VCCL. Connection to VCCL should be through a 10K resistor.*
4. *Pins with the (I/O) designator are dual function configuration pins.*
5. *All global inputs, GDIx, PCLx, and CLKx, can be used as regular I/O when the global function is not required.*

240-Pin PQFP Package

Pin Number	A65ES100 Function
1	VCCL
2	CONn
20	GND
21	VCCA
22	VCCL
28	PROBE (I/O)
31	VCCL
44	GND
45	VCCA
46	VCCL
47	TDI (I/O)
53	TMS (I/O)
61	VCCL
62	CSn
66	TCK (I/O)
71	TDO (I/O)
72	GND
73	VCCH
74	VCCL
75	VCCA
81	PCL3
83	GDI7
84	GDI6
86	CLK7
88	CLK6
90	VCCL
91	VCCA
92	GND
93	VCCA
94	CLK5
95	CLK4
97	GDI5
98	GDI4
101	PCL2
106	GND
107	VCCH
108	VCCL
109	VCCA

Pin Number	A65ES100 Function
111	A18 (I/O)
114	A17 (I/O)
117	A16 (I/O)
120	VPUMP
121	VCCL
124	A15 (I/O)
127	A14 (I/O)
131	A13 (I/O)
133	A12 (I/O)
134	VCCL
135	VCCA
136	GND
137	A11 (I/O)
140	A10 (I/O)
144	A9 (I/O)
148	A8 (I/O)
150	VCCL
152	A7 (I/O)
154	A6 (I/O)
157	A5 (I/O)
159	A4 (I/O)
160	VCCL
161	VCCA
162	GND
164	A3 (I/O)
169	A2 (I/O)
172	CCLK (I/O)
173	A1 (I/O)
177	A0 (I/O)
180	M2
181	VCCL
182	M1
186	D0 (I/O)
188	D1 (I/O)
191	D2 (I/O)
192	VCCA
193	VCCH
194	VCCL

Pin Number	A65ES100 Function
195	GND
196	D3 (I/O)
199	PCL1
201	GDI3
202	GDI2
204	CLK3
206	CLK2
208	VCCA
209	GND
210	VCCA
211	VCCL
212	GND
214	CLK1
215	CLK0
218	GDI1
219	GDI0
220	CSOUTn (I/O)
221	PCL0
223	D4 (I/O)
224	VCCA
225	VCCH
226	VCCL
227	GND
228	FRAME_CLK
229	D5 (I/O)
230	D6 (I/O)
233	ERRORn (I/O)
234	D7 (I/O)
240	M0